

WHAT IS CLAIMED IS

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1. A signal multiplexing circuit,
comprising:

10 a first selector circuit which multiplexes
two data signals in synchronization with a first
clock signal;

a second selector circuit which
multiplexes two data signals in synchronization with
a second clock signal; and

15 a clock control circuit which generates
the first clock signal and the second clock signal
as signals having a 90-degree phase shift relative
to each other.

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2. The signal multiplexing circuit as
claimed in claim 1, further comprising a third
selector circuit which multiplexes an output of said
25 first selector circuit and an output of said second
selector circuit in synchronization with a third
clock signal.

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3. The signal multiplexing circuit as
claimed in claim 2, wherein said clock control
circuit generates the first clock signal and the
35 second clock signal from the third clock signal such
that the first clock signal and the second clock
signal have half a frequency of the third clock

signal.

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4. The signal multiplexing circuit as claimed in claim 3, wherein said clock control circuit includes:

10 a first latch circuit which receives the third clock signal as a clock input; and

a second latch circuit which receives the third clock signal as a reversed clock input, and receives an output of said first latch circuit as data input,

15 wherein an inverse of an output of said second latch circuit is input into said first latch circuit as data input, the first clock signal being the output of said first latch circuit, and the second clock signal being the output of said second
20 latch circuit.

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5. The signal multiplexing circuit as claimed in claim 3, wherein said clock control circuit includes:

30 a circuit which generates the first clock signal by dividing a frequency of the third clock signal by half; and

a delay circuit which delays the first clock signal by a predetermined time length.

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6. The signal multiplexing circuit as

claimed in claim 3, further comprising:

a first data-timing adjustment circuit which shifts phases of the two data signals input into said first selector circuit; and

5 a second data-timing adjustment circuit which shifts phases of the two data signals input into said second selector circuit.

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7. The signal multiplexing circuit as claimed in claim 6, wherein said first data-timing adjustment circuit attends to timing adjustment based on the first clock signal, and said second data-timing adjustment circuit attends to timing adjustment based on the second clock signal.

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8. A transmitter for an optical communication system, comprising:

a signal multiplexing circuit;

25 an amplifier which amplifies an output of said signal multiplexing circuit; and

a modulator which modulates an optical signal according to an output of said amplifier, wherein said signal multiplexing circuit includes:

30 a first selector circuit which multiplexes two data signals in synchronization with a first clock signal;

a second selector circuit which multiplexes two data signals in synchronization with a second clock signal; and

35 a clock control circuit which generates the first clock signal and the second clock signal

as signals having a 90-degree phase shift relative to each other.

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9. The transmitter as claimed in claim 8, wherein said signal multiplexing circuit further includes a third selector circuit which multiplexes
10 an output of said first selector circuit and an output of said second selector circuit in synchronization with a third clock signal.

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10. The transmitter as claimed in claim 8, wherein said clock control circuit generates the first clock signal and the second clock signal from
20 the third clock signal such that the first clock signal and the second clock signal have half a frequency of the third clock signal.